To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim elements. Furthermore, "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art." *See* M.P.E.P. § 2143.01 (8th Ed., Aug. 2001), quoting *In re Wilson*, 424 F.2d 1382, 1385, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or to combine reference teachings. Finally, there must be a reasonable expectation of success. *See* M.P.E.P. § 2143 (8th Ed. 2001), pp. 2100-122 to 127.

The Examiner did not establish a *prima facie* case of obviousness because Doing et al and APA, either taken alone or in combination, do not teach each and every element of Applicant's invention.

**I. Claims 1, 9, 17, and 25**

Claim 1 recites a combination of steps including periodically interrupting execution of all of the threads, determining whether register data corresponding to a selected thread has changed from a previous interrupt of all of the threads of a program, and providing an indication of the change for the selected thread.

In contrast, Doing et al. discloses a multithread processor capable of switching execution between two threads of instructions and thread switch logic whereby processing of various threads of instructions allows optimization of the use of the processor among the threads. Contrary to the Examiner's assertions, Doing et al. does

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not teach or suggest a method time profiling multiple threads, as recited in claim 1. Instead, Doing et al. allows a processor to execute instruction threads to increase processor utilization during idle operations.

Specifically, the Examiner has mischaracterized the "profil[ing]" aspect of the procedure disclosed in Doing et al. The "profiling" features disclosed in Doing et al. are directed toward monitoring the performance of a software program to determine optimal values for placement in thread switching control registers. To determine these optimal values, Doing et al. executes a target program several times with varying control register values. The value corresponding to the system's best performance (e.g., the lowest cycles per instruction) is selected and stored in the register. Id. at col. 6, lines 49-67. Further, Doing et al. describes switching between threads in response to a time-out signal generated by a time-out counter. The counter tracks the number of cycles an active thread repeats when the thread is unable to execute and generates a time-out signal when a predetermined threshold value is reached. These features have no relationship with the time profiling method recited in claim 1.

Furthermore, Doing et al. does not teach or suggest, among other things, determining whether register data has changed and providing an indication of the change. Instead, the thread state register described by Doing et al., and cited by the Examiner, simply stores the state of the corresponding thread. Doing et al. does not determine whether register data for a selected thread has changed from a previous interrupt. In fact, the state register consists of bits that merely describe the current state of a thread. For example, bits 1 and 2 indicate whether the requested information is

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unavailable, and if so, from what source. Simply put, bits 1 and 2 track the type of cache misses that may have occurred during execution of a program. Similarly, bit 3 indicates whether the cache misses results in a thread switch. Therefore, Doing et al. does not teach or suggest determining whether register data corresponding to a selected thread has changed, as recited in claim 1.

Moreover, Doing et al. does not teach providing an indication of the determined change, as recited in claim 1. The thread state registers, referred to by the Examiner, identify whether the reason for a stalled execution results from a request for instructions or data. The thread state registers further identify the source of unavailable requested information, such as from a translation lookaside buffer, an L1 cache, or an L2 cache. That is, the thread state registers merely identify the state of a thread at certain points during execution of a program. These register, and any other component taught by Doing et al., do not provide an indication of a change for a selected thread, as recited in claim 1.

Further, APA does not cure the above noted deficiencies of Doing et al. Accordingly, Doing et al. and APA, either alone or in combination, do not teach or suggest each and every element of claim 1, and Applicant respectfully requests that the rejection of this claim under 35 U.S.C. § 103(a) be withdrawn and the claim allowed.

Claims 2-4, 26, and 27 depend from claim 1. As explained, claim 1 is distinguishable from Doing et al. and APA. Accordingly, claims 2-4, 26, and 27 are also distinguishable from these references for at least the same reasons set forth for claim 1.

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Further, Doing et al. does not teach or suggest comparing stored data corresponding to the selected thread with register information following a previous interrupt, as recited in claim 2. Instead, the reference describes processes for remedying situations where a thread repeatedly switches threads without executing an instruction. These processes reset a counter and compare thread states when a thread changes states and an instruction has been executed. Id. at col. 17, lines 15-35. If, on the other hand, a thread changes state and an instruction has not been executed, Doing et al. increments the counter and compares the counter's value to a threshold value. Thus, the "comparison" features taught by Doing et al. are associated with monitoring switching states of different threads, and do not teach or suggest comparing stored data with register information following a previous interrupt, as recited in claim 2.

Also, Doing et al. does not teach or suggest computing a value corresponding to the stored data and determining a relationship between the computed value and the previously stored register information, as recited in claim 3. The Examiner alleges that these recitations are taught by Doing et al. at col. 18, lines 12-40. Applicant respectfully disagrees and points out that the Examiner has taken the reference out of context. The cited text describes blocking schemes to prevent a system from repeatedly switching between threads when an instruction fails to complete during execution of a program by performing a forward progress count process. According to this process, Doing et al. allows an arbitrary number of thread switches (e.g., five) before preventing further the thread from switching to another thread. See id. at col. 17, lines 58 - col. 18, line 30. Accordingly, Doing et al. does not teach or suggest computing a value corresponding to

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stored data and determining a relationship between the computed value and the previously stored register information, as recited in claim 3.

Further, Doing et al. does not teach or suggest updating a memory segment to reflect that the selected thread is running when it is determined that the computed value and the previously stored register value do not match, as recited in claim 4. In referring to Doing et al. ("updating a memory page table" at col. 15, line 53), the Examiner has again mischaracterized the teachings of the reference. The updating of a memory page table refers to an exemplary instance where a background thread retains ownership of a single owned resource (e.g., the memory page table) for an extended period of time while another active thread requires access to the resource Accordingly, Doing et al. does not teach or suggest updating a memory segment, as recited in claim 4.

Additionally, Doing et al. does not teach or suggest assigning a cost indicator to an identified portion of the program that is active when it is determined that the selected thread is running, as recited in claim 26. The states of a thread disclosed by Doing et al., and cited by the Examiner merely represents various status states of the thread during program execution, such as a "ready" state, where a thread is ready for processing data. Accordingly, Doing et al. does not teach or suggest assigning a cost indicator, as recited in claim 26.

Doing et al. also does not teach or suggest the a cost indicator that reflects a number of cycles the selected thread was running in the identified portion of the program, as recited in claim 27. The problem of allocating processing cycles among thread disclosed in Doing et al., and cited by the Examiner, refers to situations where

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one thread may encounter long latency switch events compared to other threads, thus allowing the one thread to have more than its fair share of processing cycles. Allocating processing cycles, as taught by Doing et al. is not the same as assigning a cost indicator that reflects a number of cycles a selected thread was running in the context of claim 27.

Moreover, APA does not cure the above deficiencies of Doing et al. with respect to claims 2-4, 26, and 27 because the APA merely describes a process for periodically interrupting execution of threads in a running program. Because Doing et al. and APA, either taken alone or in combination, do not teach or suggest the recitations of claims 2-4, 26, and 27, Applicant respectfully requests that the rejection of these claims under 35 U.S.C. § 103(a) be withdrawn and the claims allowed.

Claims 9, 17, and 25 include recitations similar to those of claim 1. As explained, claim 1 is distinguishable from Doing et al. and APA. Accordingly, claims 9, 17, and 25 are also distinguishable from these references, and Applicant respectfully requests that the rejection of these claims under 35 U.S.C. § 103(a) be withdrawn and the claims allowed.

Claims 10-12, and 18-20 depend from claims 9 and 17, respectively. As explained, claims 9 and 17 are distinguishable from Doing et al. and APA. Accordingly, claims 10-12 and 18-20 are also distinguishable from these references for at least the same reasons set forth in connection with claims 9 and 17. Further, claims 10-12 and 18-20 include recitations similar to those of claims 2-4, respectively. As discussed above, claims 2-4 are also distinguishable from Doing et al. and APA. Therefore, claims

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10-12 and 18-20 are also distinguishable from these references for at least the same reasons set forth for claims 2-4, and Applicant respectfully requests that the rejection of claims 10-12 and 18-20 under 35 U.S.C. § 103(a) be withdrawn and the claims allowed.

Furthermore, claims 30 and 31 include recitations similar to claims 26 and 27, respectively. As explained, claims 26 and 27 are distinguishable from Doing et al. and APA. Accordingly, claims 30 and 31 are also distinguishable from these references for at least the same reasons set forth for claims 26 and 27, and Applicant respectfully requests that the rejection of claims 30 and 31 under 35 U.S.C. § 103(a) be withdrawn and the claims allowed.

**II. Claims 5, 13, and 21**

Claim 5 includes recitations similar to those of claims 1 and 3. As explained, claims 1 and 3 are distinguishable from Doing et al. and APA. Accordingly, claim 5 is also distinguishable from these references for at least the same reasons set forth for claims 1 and 3, and Applicant respectfully requests that the rejection of claim 5 under 35 U.S.C. § 103(a) be withdrawn and the claim allowed.

Further, **the Examiner did not address all of the recitations of claim 5**. For example, claim 5 recites a combination of steps including, at least, providing an indication corresponding to a portion of the program containing the selected thread. This step is not recited in claim 1 and is not addressed in the Office Action. Further, Doing et al. and APA, either taken alone or in combination, do not teach or suggest this recitation. Accordingly, because the Examiner failed to address, and Doing et al. and

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APA, either taken alone or in combination, do not teach or suggest, every recitation of claim 5, Applicant respectfully requests that the rejection of this claim under 35 U.S.C. § 103(a) be withdrawn and the claim allowed.

Claims 6 and 28 depend from claim 5. As explained, claim 5 is distinguishable from Doing et al. and APA. Accordingly, claims 6 and 28 are also distinguishable from these references for at least the same reasons set forth in connection with claim 5. Further, claims 6 and 28 include recitations similar to claims 4 and 27, respectively. As explained, claims 4 and 27 are distinguishable from Doing et al. and APA. Accordingly, claims 6 and 28 are also distinguishable from these references for at least the same reasons set forth for claims 4 and 27, and Applicant respectfully requests that the rejection of these claims under 35 U.S.C. § 103(a) be withdrawn and the claims allowed.

Claims 13 and 21 include recitations similar to those of claim 5. As explained, claim 5 is distinguishable from Doing et al. and APA. Accordingly, claims 13 and 21 are also distinguishable from these references for at least the same reasons set forth for claim 5, and Applicant respectfully requests that the rejection of these claims under 35 U.S.C. § 103(a) be withdrawn and the claims allowed.

Claims 14, 15 and 22, 32 depend from claims 13 and 21, respectively. As explained, claims 13 and 21 are distinguishable from Doing et al. and APA. Accordingly, claims 14, 15, 22, and 32 are also distinguishable from these references for at least the same reasons set forth in connection with claims 13 and 21, and

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Applicant respectfully requests that the rejection of these claims under 35 U.S.C. § 103(a) be withdrawn and the claims allowed.

Additionally, Doing et al. does not teach or suggest providing an indication corresponding to a portion of the program containing the selected thread, as recited in claim 15. The states of a thread disclosed by Doing et al., and cited by the Examiner merely represents various status states of the thread during program execution, such as a "ready" state, where a thread is ready for processing data. Accordingly, Doing et al. does not teach or suggest an indication corresponding to a portion of the program containing the selected thread, as recited in claim 15.

**III. Claims 8, 16, and 24**

Claims 8, 16, and 24, include recitations similar to those of claim 1. As explained, claim 1 is distinguishable from Doing et al. and APA. Accordingly, claims 8, 16, and 24 are also distinguishable from these references for at least the same reasons set forth in connection with claim 1, and Applicants request that the rejection of these claims under 35 U.S.C. § 103(a) be withdrawn and the claims allowed.

Claims 29 and 33 depend from claims 8 and 24, respectively. As explained, claims 8 and 24 are distinguishable from Doing et al. and APA. Accordingly, claims 29 and 33 are also distinguishable from these references for at least the same reasons set forth in connection with claims 8 and 24, and Applicant respectfully requests that the rejection of claims 29 and 33 under 35 U.S.C. § 103(a) be withdrawn and the claims allowed.

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**Conclusion**

In view of the foregoing remarks, Applicant requests the Examiner's reconsideration and reexamination of the application, and the timely allowance of pending claims 1-6, 8-22, and 24-33.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: May 2, 2003

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